

A Monolithic active pixel sensor for ionizing radiation using a 180nm HV-SOI process

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Abstract

An improved SOI-MAPS (Silicon On Insulator Monolithic Active Pixel Sensor) for ionizing radiation based on thick-film High Voltage SOI technology (HV-SOI) has been developed. Similar to existing Fully Depleted SOI-based (FD-SOI) MAPS, a buried silicon oxide inter-dielectric (BOX) layer is used to separate the CMOS electronics from the handle wafer which is used as a depleted charge collection layer. FD-SOI MAPS suffer from radiation damage such as transistor threshold voltage shifts due to charge traps in the oxide layers and charge states created at the silicon oxide boundaries (back gate effect). The X-FAB 180-nm HV-SOI technology offers an additional isolation by deep non-depleted implant between the BOX layer and the active circuitry which mitigates this problem. Therefore we see in this technology a high potential to implement radiation-tolerant MAPS with fast charge collection property. The design and measurement results from a first prototype are presented including charge collection in neutron irradiated samples.

Keywords: pixel, sensor, SOI, radiation hard

1. Introduction

Monolithic Active Pixel based on SOI technology has been proposed as an ultimate monolithic sensor approach for tracking detectors due to the fact that the sensor and front-end readout electronics with different requirements on silicon parameters can be integrated into a single chip [1]. Such a technology offers fabrication of devices with a large number of readout channels with fine segmentation at a small cost.

The first prototypes of an SOI-based MAPS were implemented with a FD-SOI technology [2], in which the whole body under the transistor gate is completely depleted. Unfortunately, the FD-SOI process by principle suffers significantly from Total Ionizing Dose (TID) effects [3]. Several ways have been investigated to mitigate this problem, such as extra isolating implants in the handling wafer, or the use of double SOI wafers [4].

A new commercial HV-SOI process [5], that mitigates the back gate effect problem, is being investigated. This process offers n- and p-well structures for active layers, which creates an additional isolation layer between BOX and the active circuitry making transistor parameters insensitive to radiation effects in the BOX.

To evaluate the process, we designed the prototype chip “XTB01”, which includes simple diode and readout electronics. In this article, the concept and measurement results of the prototype chip implemented with this technology are presented. The TID effects on this HV-SOI technology is reported in a separate publication [6].

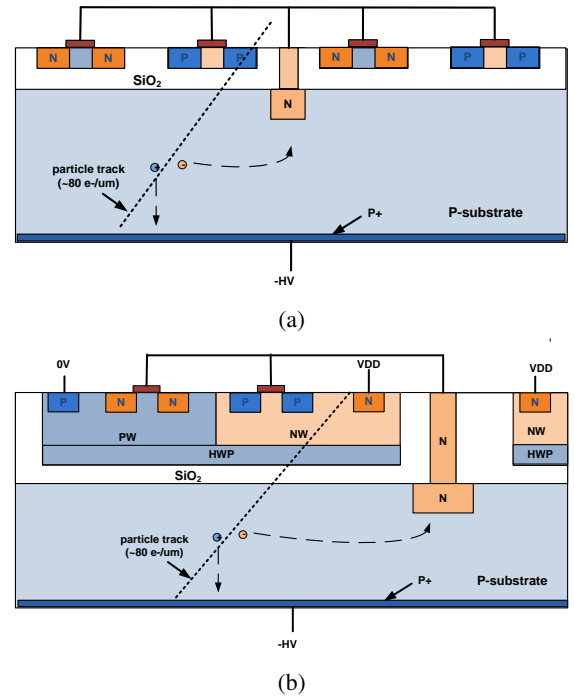


Figure 1: Cross section of a) the FD-SOI and b) the thick-film HV-SOI process for p-type silicon substrate and n-type collection diode

2. Technology Overview

A simplified cross-section of FD-SOI and thick-film SOI technologies is shown in Figure 1. In a SOI process, active devices are fabricated in a thin silicon layer on top of an insulating layer of silicon dioxide (buried oxide). The inactive layer underneath BOX (handling wafer) can be used as a depleted sensor layer. The main difference of thick-film SOI technology is that the active (transistor) layer is thick (few μm) compared to tens of nm in case of FD-SOI. Multiple biased well structures give the possibility to isolate the transistor from any influence of charge build-up in the BOX. Both technologies allow access to the handling wafer to create a charge collecting diode and bias. A standard CMOS circuit can be realized in the active layer. The process itself gives us a possibility to create high voltage (above 200V) transistors for power application. The expected depletion thickness of the handling wafer in this prototype is about 50 μm . Table 1 summarizes the technological overview.

Table 1: Overview of technological options for the prototype chip.

Features	180 nm, 4 metal layers, SOI
Supply rail	1.8V
Handling wafer type	p-type bulk with 100 $\Omega\cdot\text{cm}$
Process options	MIM capacitor, deep HV well option
Chip area	2x5 mm ²

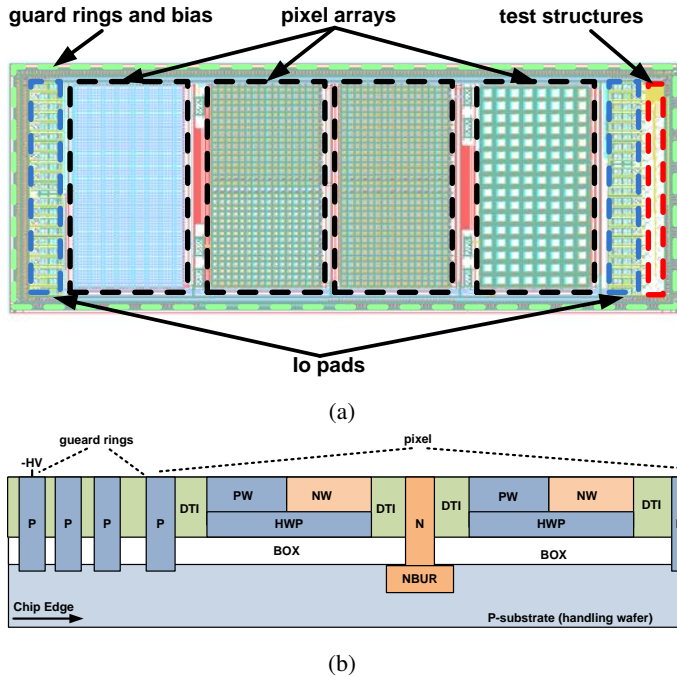


Figure 2: XTB01 prototype a) layout b) cross section

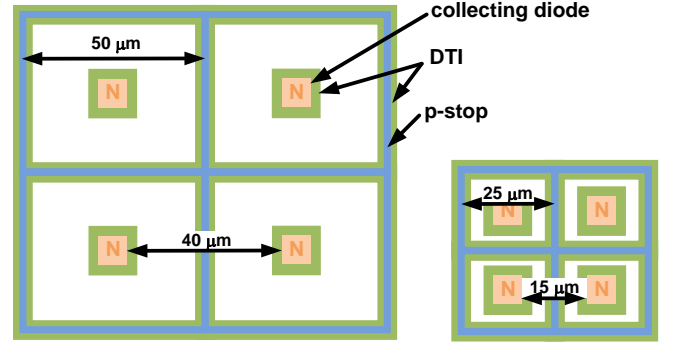


Figure 3: Pixel layout for 50 μm and 25 μm pitch pixels

3. Test Chip XTB01

To investigate the feasibility of the particle detector based on this HV-SOI technology a prototype chip XTB01 has been designed with a simple diode structure and readout scheme. The device consists of 4 pixel arrays with three different pixel sizes (25, 50, 100 μm). For the time being, no back implant is being used and thus HV bias is applied laterally. The HV ring surrounds every pixel and a multi-guard ring structure is placed next to the chip edge. A picture and cross section of the chip can be seen in Figure 2. We also implemented an array of standalone P and N type transistors, i.e., without any sensor diodes connected, at the periphery of the chip, to check immunity against radiation effects.

3.1. Pixel Design

Since the handling wafer material is p-type, n-type implants are used as a collecting electrode. The readout transistors are placed adjacent to the collecting electrode. This region is separated from the diode by deep trench isolation (DTI). The implant structures for 25 and 50 μm pixels are shown in Figure 3. P-type (p-stop) openings are placed between pixels to "break" the electron accumulation layer underneath the BOX in particular after radiation.

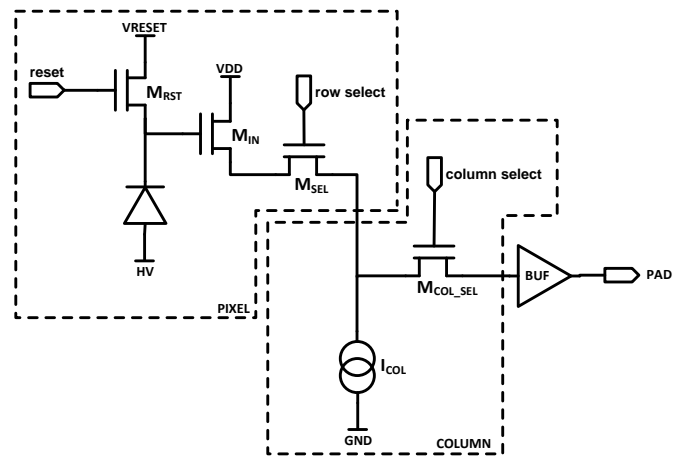


Figure 4: Block diagram of 3T pixel readout for XTB01 chip.

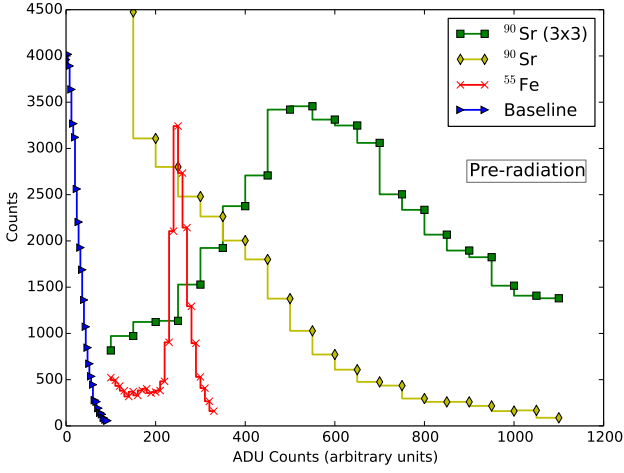


Figure 5: Single pixel spectra for 25 μm pixel from ^{55}Fe and ^{90}Sr (single pixel and 3x3 clustered) radiative source at 150V bias and -20°C .

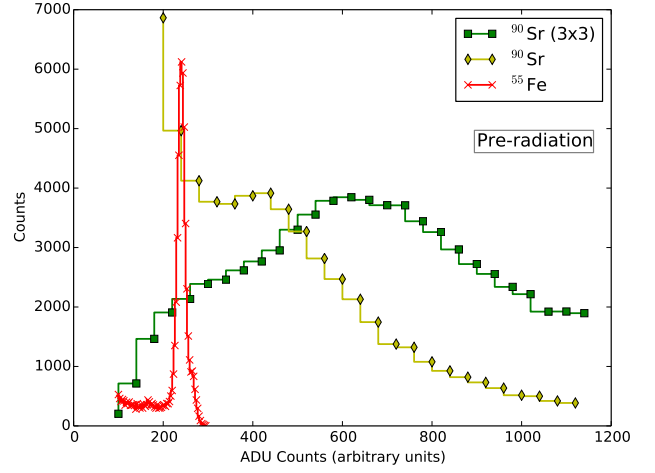


Figure 6: Single pixel spectra for 50 μm pixel from ^{55}Fe and ^{90}Sr (single pixel and 3x3 clustered) radiative source at 150V bias and -20°C .

3.2. Readout Scheme

The majority of pixels are standard three transistor (3T) pixels that allow direct access to the analog signal. This 3T readout scheme is widely used in various CMOS image sensors, and it is easy to compare sensor characteristics, such as the diode leakage current or noise performance, with other technologies. Figure 4 shows a block diagram of the 3T readout scheme [7]. The reset transistor M_{RST} is used to reset the pixel by dumping the integrated charge to the positive bias voltage. The transistor M_{SEL} is activated to select the readout of the pixel, and M_{IN} is the input transistor of a source follower. The current source is common to all the pixels in one column. A signal integrated on input capacitance is directly proportional to the charge collected and scaled by input capacitance. The control signals are provided by two shift register arrays for row and column selection. One pixel is read one at a time in rolling-shutter manner. To investigate the optimum size of the input transistors against the diode size, we added variations on transistor widths and geometries.

Table 2: Irradiation levels at different steps. (TID dose from reactor background.)

Fluence [$\text{n}_{\text{eq}}/\text{cm}^2$]	Dose [kRad]
0	0
1×10^{13}	10
5×10^{13}	50
1×10^{14}	100
5×10^{14}	500

4. Sensor performance

Spectrum measurements with radioactive sources of ^{55}Fe and ^{90}Sr have been conducted with pre-irradiated devices. Figure 5 and 6 shows the result on 25 and 50 μm pitch pixel. Based on the 5.9 keV ^{55}Fe calibration peak, the input capacitance has been estimated as ~ 15 fF (gain of $11\mu\text{V}/\text{e}$). The noise was measured at about 30 electron equivalent noise charge (ENC) at baseline. We stress that the readout is not optimized for leakage current or input capacitance. From the ^{90}Sr spectrum one can estimate for the Most Probable Value (MPV) a 3000-4000 e^- signal which suggests a collection volume of about 40-50 μm at 150 V. For all plots a threshold of 100 ADUs (700 e^-) is used for the cluster reconstruction (same in the seed and in the neighbor pixels).

4.1. Sensor performance after neutron irradiation

The chips have been irradiated in the nuclear reactor at Ljubljana with 5 different doses of neutrons. The chips were not pre-characterized. Measurements for different doses have been conducted with different devices. The neutron and TID doses are shown in Table 2. The performance of the HV-SOI pixel sensor has been studied with radioactive sources of ^{90}Sr and ^{55}Fe .

Measured I-V characteristics for an entire chip for different neutron doses at room temperature are depicted in Figure 7. With a bias voltage of 150 V on 100 $\Omega\text{-cm}$ p-type substrate we expect about 50 μm depletion thickness. We can observe a linear increase of leakage current due to defects caused by neutron damage, while the breakdown voltages are increasing. Defects could act as recombination/generation centers and are responsible for an increase of the leakage current.

Figure 8 shows a ^{90}Sr source spectrum after 10^{14} and 5×10^{14} $\text{n}_{\text{eq}}/\text{cm}^2$ for 50 μm pixel. One can observe a clustered signal of about 4000 e^- at 250 V after 10^{14} $\text{n}_{\text{eq}}/\text{cm}^2$. No signal is

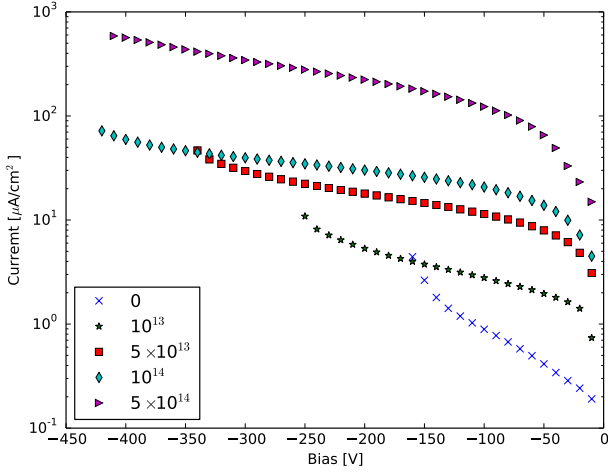


Figure 7: I-V characteristics for XTB01 for different neutron dose at 25 C°.

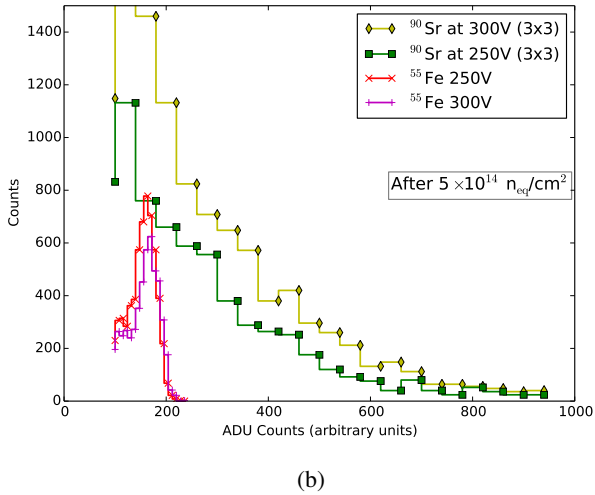
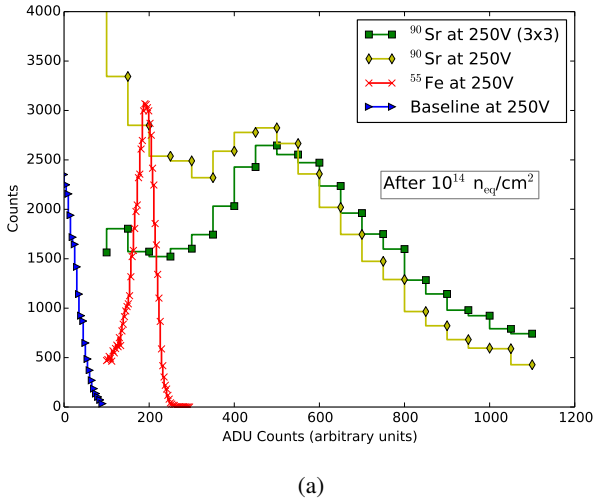


Figure 8: Single pixel spectra for ^{55}Fe and 3x3 clustered ^{90}Sr for 50 μm pixel after a) 10^{14} b) 5×10^{14} $n_{\text{eq}}/\text{cm}^2$

observed for 5×10^{14} $n_{\text{eq}}/\text{cm}^2$ which may suggest inefficiencies between pixels caused by trapping. Losing charge due to trapping between pixels may be an effect of a large distance between collecting diodes and insufficient electrical field (see Figure 3). Figure 9 shows ^{90}Sr spectrum from clustered 25 μm pixels and cluster distribution for 5×10^{14} $n_{\text{eq}}/\text{cm}^2$. Signals of about 4000 e^- are clearly seen, and this result would suggest to confirm that charge is not fully collected between pixels in case of 50 μm pixel pitch and 5×10^{14} $n_{\text{eq}}/\text{cm}^2$.

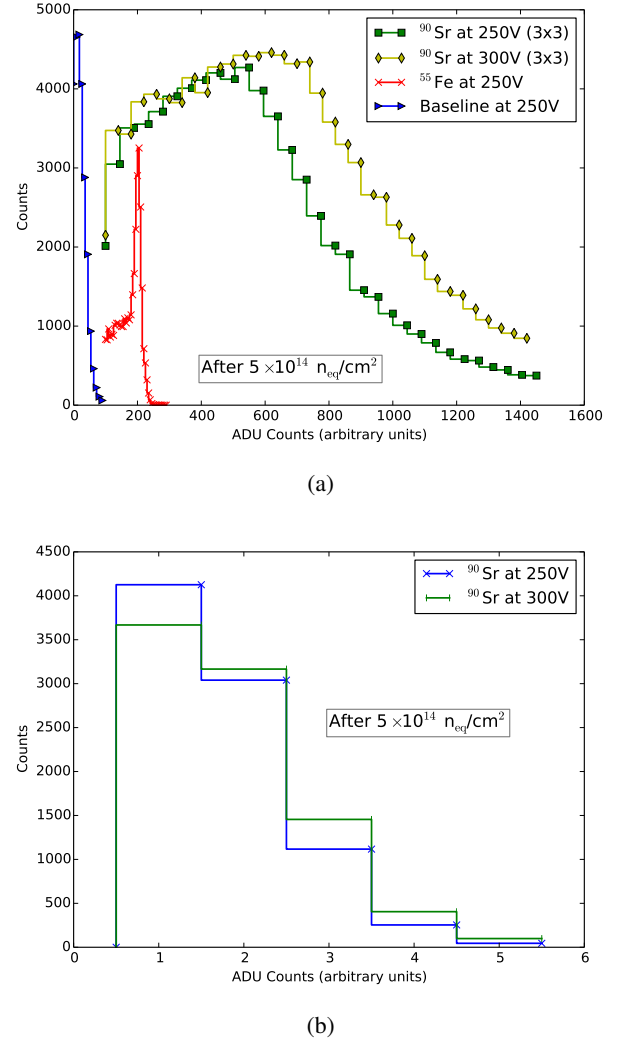


Figure 9: a) 3x3 clustered pixel ^{90}Sr and single cluster ^{55}Fe and spectra for 25 μm pixel after 5×10^{14} $n_{\text{eq}}/\text{cm}^2$ and b) ^{90}Sr cluster size distribution

5. Summary

An improved SOI-MAPS for ionizing radiation based on HV-SOI technology has been developed. In comparison to existing SOI devices, this technology makes use of thick epitaxial layer and multi-well structures to isolate transistor channels from the BOX and make them immune to the Back Gate Effects. Access

to a handling wafer below the BOX allows using the substrate as a particle sensing device. First measurements with a 100 Ω -cm handling wafer indicate that more than 200 V biased can be applied to the sensor. Signal from about 50 μ m depleted part can be collected after 5×10^{14} n_{eq}/cm^2 . Those first measurements indicate an encouraging prospect to use this technology for particle detection and tracking at radiation harsh environments. More detailed measurements are planned involving test-beam campaigns to investigate systematic studies in pixel efficiency. Comparison with TCAD simulations is also planned as a next step. A second simple passive prototype chip has been submitted for detailed investigation on different guard ring structures and pixel diode geometries, especially focusing on isolation between pixels and technological changes.

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References

- [1] M. Amati et al., "Hybrid active pixel sensors and {SOI} inspired option " Nucl. Instrum. Meth. A, 511 (2003) 265–270.
- [2] A. Bulgheroni et al., "Monolithic active pixel detector realized in silicon on insulator technology", Nucl. Instrum. Meth. A, 535 (2004) 398–403.
- [3] M. Kochiyama al., "Radiation effects in silicon-on-insulator transistors with back-gate control method fabricated with OKI Semiconductor 0.20 m FD-SOI technology", Nucl. Instrum. Meth. A, S62 (2011)
- [4] S. Honda al., "Total ionization damage effects in double silicon-on-Insulator devices", Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2013 IEEE
- [5] A. Hölke et al., "A 200V partial SOI 0.18m CMOS technology" in Proc. of 22th International Symposium on Power Semiconductor Devices and ICS (ISPSD), 2010, Japan, pp. 257-260
- [6] S. Fernandez-Perez et al., "Radiation Hardness of a 180nm SOI Monolithic Active Pixel Sensor", Nucl. Instrum. Meth. A, published in the same proceedings.
- [7] R. Turchetta et al., "A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology ", Nucl. Instrum. Meth. A, 501 (2003) 251–259.